

IN THE CLAIMS:

The status of each claim that has been introduced in the above-referenced application is identified in the ensuing listing of the claims. This listing of the claims replaces all previously submitted claims listings.

1. (Currently amended) A method for fabricating a chip-scale package, comprising:
  - positioning a sacrificial substrate adjacent to a back side of a device substrate with a plurality of conductive elements on an active surface of said the sacrificial substrate being aligned along at least one street between adjacent semiconductor devices on an active surface of said the device substrate;
  - securing said the active surface of said the sacrificial substrate to said the back side of said the device substrate with a quantity of dielectric material electrically isolating each conductive element of said the plurality of conductive elements from said the back side of said the device substrate;
  - severing said the device substrate to physically separate said the adjacent semiconductor devices from one another and to form peripheral edges of each semiconductor device of said the adjacent semiconductor devices, relative positions of said the adjacent semiconductor devices being maintained by said the sacrificial substrate;
  - forming a dielectric coating on at least portions of at least some of said the peripheral edges;
  - exposing at least portions of at least some conductive elements of said the plurality of conductive elements, each exposed conductive element comprising a lower section of a contact pad of the chip-scale package; and
  - forming a peripheral section of said the contact pad in communication with a corresponding lower section and on a peripheral edge of a semiconductor device.

2. (Currently amended) The method of claim 1, further comprising:
  - forming a redistribution layer on said the active surface of said the device substrate and in electrical isolation from circuitry of an underlying semiconductor device.

3. (Currently amended) The method of claim 2, wherein ~~said~~ forming saidthe dielectric coating includes forming a dielectric coating over at least portions of saidthe active surface of saidthe device substrate.

4. (Currently amended) The method of claim 3, wherein ~~said~~ forming the dielectric coating over at least portions of saidthe active surface of saidthe device substrate electrically isolates at least one conductive trace of saidthe redistribution layer from circuitry of an underlying semiconductor device.

5. (Currently amended) The method of claim 2, wherein ~~said~~ forming saidthe redistribution layer is effected before ~~said~~ severing.

6. (Currently amended) The method of claim 5, wherein ~~said~~ severing includes severing at least one conductive trace of saidthe redistribution layer.

7. (Currently amended) The method of claim 2, further comprising: forming an upper section of saidthe contact pad in communication with both saidthe peripheral section and a conductive trace of saidthe redistribution layer and over at least one semiconductor device of saidthe adjacent semiconductor devices.

8. (Currently amended) The method of claim 1, further comprising: forming an upper section of saidthe contact pad in communication with saidthe peripheral section and over at least one semiconductor device of saidthe adjacent semiconductor devices.

9. (Currently amended) The method of claim 1, further comprising: removing at least a portion of saidthe sacrificial substrate to facilitate separation of saidthe adjacent semiconductor devices from one another.

10. (Currently amended) The method of claim 9, wherein ~~said~~-removing comprises substantially removing saidthe sacrificial substrate.

11. (Currently amended) The method of claim 10, wherein ~~said~~-substantially removing comprises back grinding saidthe sacrificial substrate.

12. (Currently amended) The method of claim 1, wherein ~~said~~-securing comprises use of a dielectric adhesive material.

13. (Currently amended) The method of claim 1, wherein ~~said~~-severing is effected into saidthe dielectric material.

14. (Currently amended) The method of claim 1, wherein ~~said~~-forming saidthe dielectric coating comprises introducing dielectric material into at least one recess formed ~~during~~ saidby severing.

15. (Currently amended) The method of claim 14, wherein ~~said~~-introducing comprises forming a layer comprising saidthe dielectric material over at least a portion of saidthe active surface of saidthe device substrate.

16. (Currently amended) The method of claim 14, wherein ~~said~~-introducing comprises introducing a dielectric polymer into saidthe at least one recess.

17. (Currently amended) The method of claim 14, wherein ~~said~~-introducing comprises substantially filling saidthe at least one recess with saidthe dielectric material.

18. (Currently amended) The method of claim 17, further comprising severing saidthe dielectric material to re-separate saidthe adjacent semiconductor devices from one another.

19. (Currently amended) The method of claim 18, wherein ~~said~~ exposing is effected substantially concurrently with ~~said~~ severing ~~said~~the dielectric material.

20. (Currently amended) The method of claim 1, wherein ~~said~~ positioning comprises positioning ~~said~~the device substrate such that ~~said~~the at least one street is aligned over at least some conductive elements of ~~said~~the plurality of conductive elements.

21. (Currently amended) The method of claim 20, wherein ~~said~~ exposing comprises severing ~~said~~the at least some conductive elements.

22. (Currently amended) The method of claim 1, wherein ~~said~~ positioning comprises positioning ~~said~~the device substrate such that ~~said~~the at least one street is aligned between an adjacent pair of conductive elements of ~~said~~the plurality of conductive elements.

23. (Currently amended) The method of claim 1, further comprising: forming a temporary protective layer over at least a portion of each of ~~said~~the adjacent semiconductor devices prior to ~~said~~ forming ~~said~~the dielectric coating.

24. (Currently amended) The method of claim 23, wherein ~~said~~ forming ~~said~~the temporary protective layer is effected prior to ~~said~~ severing.

25. (Currently amended) The method of claim 23, wherein ~~said~~ forming ~~said~~the temporary protective layer comprises forming ~~said~~the temporary protective layer over an optical element comprising at least one of a sensing area and an emission area of each semiconductor device of ~~said~~the adjacent semiconductor devices.

26. (Currently amended) The method of claim 25, further comprising: forming a redistribution layer over saidthe active surface, at least one conductive trace of saidthe redistribution layer extending at least partially over at least one semiconductor device of saidthe adjacent semiconductor devices.

27. (Currently amended) The method of claim 25, further comprising: removing saidthe temporary protective layer.

28. (Currently amended) The method of claim 27, further comprising: positioning an optically transparent lid over saidthe optical element of at least one semiconductor device of saidthe adjacent semiconductor devices.

29. (Currently amended) The method of claim 28, wherein said-positioning saidthe optically transparent lid comprises positioning an optically transparent lid over optical elements of a plurality of saidthe adjacent semiconductor devices.

30. (Currently amended) The method of claim 29, further comprising: severing saidthe optically transparent lid to form an individual optically transparent lid over each of saidthe optical elements.

31. (Currently amended) The method of claim 30, wherein said-severing saidthe optically transparent lid is effected substantially concurrently with said-exposing at least portions of at least some conductive elements.

32. (Currently amended) The method of claim 30, wherein said-severing saidthe optically transparent lid comprises forming saidthe individual optically transparent lid to include a peripheral edge that comprises at least one of a bevel and a chamfer.

33. (Currently amended) The method of claim 30, wherein ~~said-forming~~ saidthe dielectric coating comprises severing dielectric material within at least one recess between saidthe adjacent semiconductor devices ~~following~~ after severing saidthe optically transparent lid.

34. (Currently amended) The method of claim 28, wherein ~~said-positioning~~ saidthe optically transparent lid comprises positioning an individual optically transparent lid over at least saidthe optical element of saidthe at least one semiconductor device, saidthe individual optically transparent lid not extending over another semiconductor device of saidthe adjacent semiconductor devices.

35. (Currently amended) The method of claim 28, further comprising:  
forming a sacrificial layer over saidthe optically transparent lid.

36. (Currently amended) The method of claim 35, wherein ~~said-forming~~ saidthe peripheral section of saidthe contact pad comprises:  
forming a layer comprising conductive material over saidthe sacrificial layer and on saidthe peripheral edge;  
patterning saidthe layer comprising conductive material to form saidthe peripheral section; and  
removing saidthe sacrificial layer and portions of saidthe layer comprising conductive material that remain thereon.

37. (Currently amended) The method of claim 36, wherein ~~said-removing~~ comprises lifting saidthe portions off of saidthe optically transparent lid.

38-64 (Canceled)

65. (Currently amended) A method for assembling a chip-scale package with another semiconductor device component, comprising:

orienting the chip-scale package ~~at least partially over an upper surface of adjacent to~~ the another semiconductor device component ~~with a back side of the chip-scale package facing said upper surface of the another semiconductor device component~~, the chip-scale package including a plurality of contacts corresponding to a plurality of contacts of the semiconductor device component, at least some contacts of ~~said~~the plurality of contacts of the chip-scale package including at least ~~peripheral~~ sections on an outer periphery of the chip-scale package that extend along an entire height of the outer periphery of the chip-scale package; and

disposing intermediate conductive elements between at least some contacts of ~~said~~the plurality of contacts of the chip-scale package and corresponding contacts of ~~said~~the plurality of contacts of the semiconductor device component.

66. (Currently amended) The method of claim 65, wherein ~~said~~-orienting comprises orienting the chip-scale package at least partially over ~~said~~the upper surface of the another semiconductor device component such that ~~said~~the corresponding contacts of the another semiconductor device component are exposed beyond ~~said~~the outer periphery of the chip-scale package and ~~said~~-disposing comprises disposing ~~said~~the intermediate conductive elements between ~~said~~the peripheral sections of ~~said~~the at least some contacts and ~~said~~the corresponding contacts.

67. (Currently amended) The method of claim 65, wherein ~~said~~-orienting comprises orienting the chip-scale package at least partially over ~~said~~the upper surface of the another semiconductor device component such that ~~said~~the corresponding contacts of the another semiconductor device component are located beneath the chip-scale package and ~~said~~-disposing comprises disposing ~~said~~the intermediate conductive elements between lower sections of ~~said~~the at least some contacts extending over portions of a back side of the chip-scale package and ~~said~~the corresponding contacts.

68. (New) A method for assembling a chip-scale package with another semiconductor device component, comprising:  
orienting a chip-scale package with contacts that include at least peripheral sections on an outer periphery of the chip-scale package at least partially over another semiconductor device component such that corresponding contacts of the another semiconductor device component are exposed beyond the outer periphery of the chip-scale package; and  
disposing intermediate conductive elements between the peripheral sections of the contacts of the chip-scale package and corresponding contacts of the plurality of contacts of the semiconductor device component.

69. (New) A method for fabricating a chip-scale package, comprising:  
forming a redistribution layer on the active surface of a device substrate and in electrical isolation from circuitry of at least one underlying semiconductor device;  
positioning a sacrificial substrate adjacent to a back side of the device substrate with a plurality of conductive elements on an active surface of the sacrificial substrate being aligned along at least one street between adjacent semiconductor devices on an active surface of the device substrate;  
securing the active surface of the sacrificial substrate to the back side of the device substrate with a quantity of dielectric material electrically isolating each conductive element of the plurality of conductive elements from the back side of the device substrate;  
severing the device substrate to physically separate the adjacent semiconductor devices from one another and to form peripheral edges of each semiconductor device of the adjacent semiconductor devices, relative positions of the adjacent semiconductor devices being maintained by the sacrificial substrate;  
forming a dielectric coating on at least portions of at least some of the peripheral edges;  
exposing at least portions of at least some conductive elements of the plurality of conductive elements, each exposed conductive element comprising a lower section of a contact pad of the chip-scale package; and

forming a peripheral section of the contact pad in communication with a corresponding lower section and on a peripheral edge of a semiconductor device.

70. (New) The method of claim 69, wherein forming the dielectric coating includes forming a dielectric coating over at least portions of the active surface of the device substrate.

71. (New) The method of claim 70, wherein forming the dielectric coating over at least portions of the active surface of the device substrate electrically isolates at least one conductive trace of the redistribution layer from circuitry of an underlying semiconductor device.

72. (New) The method of claim 69, wherein forming the redistribution layer is effected before severing.

73. (New) The method of claim 72, wherein severing includes severing at least one conductive trace of the redistribution layer.

74. (New) The method of claim 69, further comprising:  
forming an upper section of the contact pad in communication with both the peripheral section and a conductive trace of the redistribution layer and over at least one semiconductor device of the adjacent semiconductor devices.

75. (New) The method of claim 69, further comprising:  
forming an upper section of the contact pad in communication with the peripheral section and over at least one semiconductor device of the adjacent semiconductor devices.

76. (New) The method of claim 69, further comprising:  
removing at least a portion of the sacrificial substrate to facilitate separation of the adjacent semiconductor devices from one another.

77. (New) The method of claim 76, wherein removing comprises substantially removing the sacrificial substrate.

78. (New) The method of claim 77, wherein substantially removing comprises back grinding the sacrificial substrate.

79. (New) The method of claim 69, wherein securing comprises use of a dielectric adhesive material.

80. (New) The method of claim 69, wherein severing is effected into the dielectric material.

81. (New) The method of claim 69, wherein forming the dielectric coating comprises introducing dielectric material into at least one recess formed during severing.

82. (New) The method of claim 81, wherein introducing comprises forming a layer comprising the dielectric material over at least a portion of the active surface of the device substrate.

83. (New) The method of claim 81, wherein introducing comprises introducing a dielectric polymer into the at least one recess.

84. (New) The method of claim 81, wherein introducing comprises substantially filling the at least one recess with the dielectric material.

85. (New) The method of claim 84, further comprising: severing the dielectric material to re-separate the adjacent semiconductor devices from one another.

86. (New) The method of claim 85, wherein exposing is effected substantially concurrently with severing the dielectric material.

87. (New) The method of claim 69, wherein positioning comprises positioning the device substrate such that the at least one street is aligned over at least some conductive elements of the plurality of conductive elements.

88. (New) The method of claim 87, wherein exposing comprises severing the at least some conductive elements.

89. (New) The method of claim 69, wherein positioning comprises positioning the device substrate such that the at least one street is aligned between an adjacent pair of conductive elements of the plurality of conductive elements.

90. (New) The method of claim 69, further comprising:  
forming a temporary protective layer over at least a portion of each of the adjacent semiconductor devices prior to forming the dielectric coating.

91. (New) The method of claim 90, wherein forming the temporary protective layer is effected prior to severing.

92. (New) The method of claim 91, wherein forming the temporary protective layer comprises forming the temporary protective layer over an optical element comprising at least one of a sensing area and an emission area of each semiconductor device of the adjacent semiconductor devices.

93. (New) The method of claim 92, further comprising:  
removing the temporary protective layer.

94. (New) The method of claim 93, further comprising:  
positioning an optically transparent lid over the optical element of at least one semiconductor device of the adjacent semiconductor devices.

95. (New) The method of claim 94, wherein positioning the optically transparent lid comprises positioning an optically transparent lid over optical elements of a plurality of the adjacent semiconductor devices.

96. (New) The method of claim 95, further comprising:  
severing the optically transparent lid to form an individual optically transparent lid over each of the optical elements.

97. (New) The method of claim 96, wherein severing the optically transparent lid is effected substantially concurrently with exposing at least portions of at least some conductive elements.

98. (New) The method of claim 96, wherein severing the optically transparent lid comprises forming the individual optically transparent lid to include a peripheral edge that comprises at least one of a bevel and a chamfer.

99. (New) The method of claim 96, wherein forming the dielectric coating comprises severing dielectric material within at least one recess between the adjacent semiconductor devices after severing the optically transparent lid.

100. (New) The method of claim 94, wherein positioning the optically transparent lid comprises positioning an individual optically transparent lid over at least the optical element of the at least one semiconductor device, the individual optically transparent lid not extending over another semiconductor device of the adjacent semiconductor devices.

101. (New) The method of claim 94, further comprising:  
forming a sacrificial layer over the optically transparent lid.

102. (New) The method of claim 101, wherein forming the peripheral section of the contact pad comprises:

forming a layer comprising conductive material over the sacrificial layer and on the peripheral edge;  
patterning the layer comprising conductive material to form the peripheral section; and  
removing the sacrificial layer and portions of the layer comprising conductive material that remain thereon.

103. (New) The method of claim 102, wherein removing comprises lifting the portions off of the optically transparent lid.